REMARKS

Applicants appreciate the examination of the application that is evidenced by the Official Action of December 7, 2005. In response to this Official Action, Applicants have canceled Claims 1-6, 9-13 and 18-20. Claims 7, 14 and 17 have also been amended. Applicants will now address the substantive rejections based on Applicants' admitted prior art and U.S. Patent No. 6,424,659 to Viswanadham et al.

The Pending Claims are Patentable Over the Cited Prior Art

Applicants respectfully request reconsideration of the outstanding rejections of the pending claims because the Examiner's interpretation of the '659 patent to Viswanadham is incorrect. To highlight this error, Applicants will first discuss the disclosure of the '659 patent and then describe the subject matter of the pending claims.

1. The '659 Patent Describes "CPU-Controlled" Aging

As described at Cols. 17-19 of the '659 patent to Viswanadham, the age table maintenance function performed by the L3 Search Engine **70** in FIG. 14 includes:

1. Maintaining an age table in control memory 136;
2. Adding and deleting entries in the age table by CPU 12 request;
3. Aging the table at CPU-controlled intervals;
4. Reporting aged entries to CPU;
5. Maintaining an aging time stamp; and
6. Making entries live.

(See, '659 patent, Col. 17, lines 4-9).

This list shows that the aging "table" is aged by the CPU at CPU-controlled intervals. In other words, it is the CPU, not the L3 Search Engine **70**, that controls when aging operations are to be performed. This CPU control is further described at Col. 18 of the '659 patent:

"CPU adds entry to age table [in L3 Search Engine] when

creating new entry in LE CAM. Until entry is added to age table, entry does not participate in aging process. CPU 12 writes (e.g., AgeCmd) register with entry number and add or add permanent command, and hardware reads appropriate entry, modifies valid and permanent bits appropriately and writes currTIME into time stamp field.

Hardware makes entry live (i.e., accessed) when L3 CAM lookup results in IP hit. Entry number of matching entry is used to access age table, and time stamp field is updated within currTime. Entries which are accessed frequently have more recent time stamp than infrequently used entries, and are not aged out.

CPU 12 deletes entry in age table when removing entry from L3 CAM 126. CPU 12 writes AgeCmd register with entry number and delete command, and hardware reads appropriate entry, clears valid bit, and writes modified entry back to table.

When CPU 12 age timer expires, CPU writes AgeCmd register to initiate aging process. This sets AgeCmd Busy bit in L3 Status register until entire table is aged. Add and delete commands can be issued, but new age commands have no affect.

When CPU writes AgeCmd register, hardware increments ageTime and currTime counters and resets aging address counter to zero. Hardware reads 32K words of age table and checks if any time stamp fields are equal to ageTime. Entries with time stamps equal to ageTime are reported to CPU 12 as aged out. CPU 12 deletes aged entry from CAM and age table."

(See, '659 patent, Col. 18-19, lines 53-67 and 1-14, emphasis added).

The above highlighted passages from the '659 patent reflect the high level of CPU control over the aging operations. In particular, it is the "age timer" within the CPU that causes the CPU to initiate an aging operation by writing into the AgeCmd register within the Search Engine. In response, the Search Engine reads the 32K

words from the age table in order to identify which entries in the corresponding internal CAM are too "old". This determination of age is performed by evaluating whether the time stamp for a given entry equals ageTime, which means the entry is older than the valid age allowed by the CPU. If an entry is determined as too old, the entry is deleted from the CAM and from the age table maintained within the Search Engine. Thus, it is the CPU, not the search engine, that issues the age command and controls aging operations within the search engine.

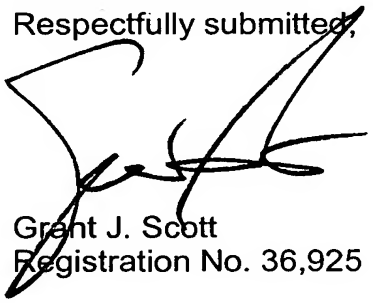
2. The Present Invention performs aging within the search engine (not under CPU control) and then Reports to the CPU after entries have been aged.

The present invention eliminates the need for a command host (e.g., CPU chip) to control aging operations within a search engine chip. In the present invention, aging operations are performed independent of CPU control. Nonetheless, after a certain number of internal aging operations have been performed, the search engine generates an interrupt, which may be provided to a command host. This interrupt tells the command host that it is time to access the search engine to obtain an upload of data (e.g., addresses) regarding entries that have been sufficiently aged. In independent Claim 7, a FIFO memory device within the search engine device is filled with addresses of aged out entries. A level count register and a level configuration register are also provided. These registers support the control circuit, which automatically issues an interrupt (e.g., to a command host (via the search engine interface)) when the FIFO capacity exceeds a threshold count value. In this manner, the CPU is notified at appropriate intervals when a sufficient number of addresses of aged out entries have been accumulated within the search engine. This may eliminate the need for the CPU to maintain an internal timer to regulate the timing of when aging inquiries are made and also may eliminate the possibility that an aging request from the CPU will result in the return of no aged-out entries. Applicants respectfully submit that the cited prior art does not disclose or suggest these aspects of Claim 7.

Finally, with respect to independent Claim 14, Applicants respectfully submit that the '659 patent does not disclose "generating an interrupt" in response to "detecting a sufficiently full storage device (e.g., FIFO) containing addresses of entries that have been aged out of the at least one database." Instead, as described above, the '659 discloses a CPU having an internal timer that decides the time interval for issuing an age command to the search engine device and the search engine device operates entirely under the control of the CPU. This is entirely contrary to the claimed control circuit, which generates an interrupt when a sufficiently full storage device (containing addresses of aged out entries) is detected within the search engine device.

Based on these arguments, Applicants respectfully submit that all pending claims are in condition for allowance, which is respectfully requested.

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 7, 2006.

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